

- 14.** An apparatus comprising:
 a three-dimensional processor stack comprising a plurality of processor cores implemented in a plurality of layers; and
 a controller to:
 generate values of thermal couplings between the plurality of layers based on temperatures measured in the plurality of layers;
 detect a thermal event at a first processor core implemented in a first layer; and
 determine whether a first thread executing on the first processor core is a critical thread based on a measure of criticality of the first thread; and
 selectively throttle at least one of the plurality of processor cores in response to detecting the thermal event, wherein the controller is to selectively throttle the at least one of a plurality of processor cores based on values of thermal couplings between the plurality of layers and based on measures of criticality of threads executing on the plurality of processor cores, wherein the controller is to selectively throttle at least one second processor core implemented in a second layer in response to the first thread being a critical thread and a second thread executing on the second processor core not being a critical thread.
- 15.** The apparatus of claim **14**, wherein the controller is to selectively throttle the at least one second processor core based on a thermal coupling between the first layer and the second layer.
- 16.** The apparatus of claim **14**, wherein the controller is to determine whether the thermal event is resolved by throttling the at least one second processor core and throttle at least one other processor core in response to the thermal event not being resolved.
- 17.** The apparatus of claim **10**, wherein the plurality of processor cores in each of the plurality of layers are to iteratively execute a predetermined code, and wherein the apparatus further comprises:
 a plurality of sensors to measure temperatures in each of the plurality of layers in response to executing the

predetermined code on the plurality of processor cores in each of the plurality of layers, and wherein the controller is to generate the values of the thermal couplings between the plurality of layers based on the measured temperatures.

18. The apparatus of claim **17**, wherein the controller is to determine values of latencies between temperature changes in each of the plurality of processor cores in each of the plurality of layers.

19. A non-transitory computer readable storage medium embodying a set of executable instructions, the set of executable instructions to manipulate a computer system to perform a portion of a process to fabricate at least part of a processor, the processor comprising:

- a three-dimensional processor stack comprising a plurality of processor cores implemented in a plurality of layers, wherein at least one of the plurality of processor cores is implemented in each of the plurality of layers; and
 - a controller to generate values of thermal couplings between the plurality of layers and selectively throttle at least one of a plurality of processor cores in response to detecting a thermal event, wherein the values of the thermal couplings indicate temperature changes in each of the plurality of layers as a function of temperature changes in each of the other layers, and wherein the controller selectively throttles the at least one of a plurality of processor cores based on the values of the thermal couplings and measures of criticality of threads executing on the plurality of processor cores.
- 20.** The non-transitory computer readable storage medium of claim **19**, wherein the processor further comprises:
 a plurality of sensors to measure temperatures in each of the plurality of layers in response to iterative execution of a predetermined code on the plurality of processor cores in each of the plurality of layers, and wherein the controller is to generate the values of the thermal couplings between the plurality of layers based on the measured temperatures.

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